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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,846	06/01/2004	Ching-Huei Tsai	NAUP0572USA	3845
27765	7590	09/19/2006	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			HU, SHOUXIANG	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/709,846

Applicant(s)

TSAI, CHING-HUEI

Examiner

Shouxiang Hu

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

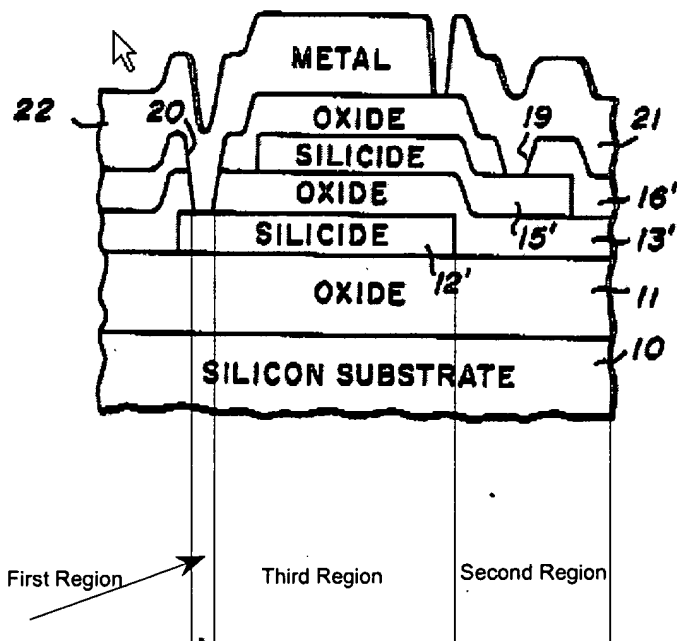
DETAILED ACTION***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Himes (Himes et al., US 4,731,696) in view of applicant's admitted prior art ("AAPA").

Himes teach a semiconductor wafer (Fig. 8, for example, as illustrated below), comprising:



a substrate with a first region (directly under the plug 20), a second region, and a third region horizontally defined on the surface of the substrate; and

a capacitor disposed on the substrate (10), the capacitor comprising: a first electrode (12') in the first region and the third region; a first isolation layer (13') on the first electrode, the first isolation (13') covering a portion of the first electrode in the third region and the substrate in the second region, but not covering the first electrode in the first region; and, a second electrode (15') on the first isolation layer, the second electrode covering the first electrode in the third region and covering the substrate in the second region.

Himes does not expressly teach that the first and second electrodes can also be formed of a polysilicon, and/or that the semiconductor wafer can further comprising a field oxide beneath the first electrode (as further recited in claims 7 and 16).

However, Himes does further teach that (col. 1, lines 8-11) polysilicon can be used to form capacitor electrode, especially when thermally grown oxide dielectric layer are employed (which require at least thermal stability). And, as evidenced in AAPA (see the first and second electrodes 16 and 22, and the field oxide layer 14 in Fig.1 of the instant disclosure; also see [0007]), one of ordinary skill in the art would readily recognize that polysilicon is one of the few commonly used material for forming capacitor electrodes in the art for the desired thermal and/or electrical stability; and/or that such field layer can be desirably formed in order to form an integrated circuit involving the capacitor and provided required insulation between the capacitor and the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Himes with the first and second electrodes being made of polysilicon, per the teachings of AAPA and/or per the further teachings of Himes, so that a device with a capacitor having desired thermal and/or electrical stability would be obtained.

Regarding claims 7 and 16, therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further incorporate the field oxide layer of AAPA into the above collectively taught device, so that device with a desirable integrated circuit involving the capacitor and/or with desired insulation between the capacitor and the substrate would be obtained.

Regarding claim 2, Himes et al. teach a semiconductor wafer, wherein the capacitor further comprises a second isolation layer (16') covering the capacitor and the substrate.

Regarding claims 3 and 12, Himes further teaches a semiconductor wafer, wherein the capacitor further comprises a first contact plug (in via 20) located in the second isolation layer and electrically connected to the first electrode.

Regarding claims 4 and 13, Himes further teaches a semiconductor wafer, wherein the first contact plug is located in the first region.

Regarding claims 5 and 14, Himes et al. teach a semiconductor wafer, wherein the capacitor further comprises a second contact plug (via 19) located in the second isolation layer and electrically connected to the second electrode.

Regarding claims 6 and 15, Himes et al. teach a semiconductor wafer, wherein the second contact plug is located in the second region.

Regarding claim 10, Himes et al. teach a semiconductor wafer, wherein the first isolation layer comprises silicon oxide.

Response to Arguments

2. Applicant's arguments filed on July 3, 2006 have been fully considered but they are not persuasive.

Responses to applicant's arguments regarding whether Himes disclose the three recited regions and their positional relationships with the other recited elements have been incorporated into the claims rejections set forth above in this office action.

And, applicant's other arguments with respect to the claims rejected above have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SH
September 12, 2006



SHOUXIANG HU
PRIMARY EXAMINER